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10/717,675	11/21/2003	Chang Su Kyeong	8734.259.00-US	9069

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EXAMINER	
SHAPIRO, LEONID	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,675	KYEONG ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-9,11,13,14 and 16* is/are rejected.

7)☒ Claim(s) *5-6,10,12,15,17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,097,362) in view of Lee (US 7,095,393).

As to claim 1, Kim teaches a driving apparatus of a liquid crystal display device (col. 1, lines 10-13), comprising:

a shift register array for sequentially generating a sampling signal (fig. 2, item 31);

a latch array for sequentially latching pixel data by designated units in response to the sampling signal to simultaneously output the latched pixel data to a first multiplexer array, the pixel data including pixel RGB data (fig. 2, item 33, col. 3, lines 41-57);

the first multiplexer array for performing time-division on inputted pixel data to supply time-divided pixel data (fig. 2, item 37, col. 3, lines 40-57);

a digital-to-analog converter array for converting the time-divided pixel data into pixel voltage signals (fig. 2, items 37,39,41 col. 3, lines 40-57); and

a demultiplexer array for driving data lines in a time-division manner to supply the converted pixel voltage signals (fig. 2, item 41, col. 3, lines 40-57),

wherein the digital-to-analog converter array receives a plurality of pixel voltage signal levels inputted from the multiplexer array and generates the pixel voltage signals using the pixel voltage signal level (fig. 2, items 37,39,41, from col. 3, line 61 to col.4,line 17).

Kim does not disclose generates a first pixel voltage signal level having a first voltage value corresponding to the first time-divided pixel data signal, generates a second pixel voltage signal level having a voltage at least one-step higher in absolute value than the original first pixel voltage signal level in correspondence to at least one and corresponding to the first time-divided pixel data and odd, even data.

Lee teaches voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data (fig.7, item 400,col. 8, lines 52-63 and col. 12. lines 1-31) and odd, even data (fig. 7, item D1-D2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Lee into Kim system in order to enhance the response speed (col. 2, lines 25-26 in the Lee reference).

As to claim 2, Kim teaches a buffer array for buffering the pixel voltage signal to supply the buffered signal to the demultiplexer array (fig. 2,item 45).

As to claim 3, Kim teaches the first multiplexer array includes at least an N-number (N is a positive integer) of multiplexers and performs time-division on a plurality of input pixel data to supply the time-divided pixel data, the digital-to-analog converter array converts the time-divided pixel data into the pixel voltage signals, and the demultiplexer array includes at least an N-number of demultiplexers and supplies the pixel voltage signals to a plurality of data lines (fig. 2, items 37,39,41, from col. 2, line 40 to col.4,line 17).

As to claim 13, Kim teaches a driving apparatus of a liquid crystal display device (col. 1, lines 10-13), comprising:

performing time-division on pixel data inputted from an external source to output time-divided RGB pixel data (fig. 2, item 37, col. 3, lines 40-57);

converting the time-divided pixel data into pixel voltage signals (fig. 2, items 37,39,41, col. 3, lines 40-57); and

performing time-division manner on data lines to supply the converted pixel voltage signals (fig. 2, item 41, col. 3, lines 40-57),

performing time-division on pixel data inputted from an external source to output time-divided pixel data (fig. 2, items 37,39,41, from col. 2, line 61 to col.4,line 17).

Kim does not disclose generating the pixel voltage signals ~ each having a first pixel voltage signal level corresponding to the first time divided pixel data and a second pixel voltage signal level having a voltage at least one step higher in absolute value

than the first an original pixel voltage signal level in correspondence to the first pixel time divided at least one pixel and odd, even data.

Lee teaches voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data (fig.7, item 400,col. 8, lines 52-63 and col. 12. lines 1-31) and odd, even data (fig. 7, item D1-D2).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Lee into Kim system in order to enhance the response speed (col. 2, lines 25-26 in the Lee reference).

3. Claims 4,7-9,11,14,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Lee as applied to claim 3 above, and further in view of Jeong (US 6,335,721 B1).

As to claim 4, Kim and Lee do not disclose at least an "N+l"-number of positive and negative digital-to-analog converters for converting the time-divided pixel data into the pixel voltage signals, wherein the positive and negative digital-to-analog converters are alternately arranged.

Jeong teaches "N "-number of positive and negative digital-to-analog converters for converting the time-divided pixel data into the pixel voltage signals, wherein the positive and negative digital-to-analog converters are alternately arranged (Fig. 4, item 500, col. 6, lines 21-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Jeong into Lee and Kim system in order to reduce number of components (col. 2, lines 51-52 in the Jeong reference).

As to claims 7-8, Jeong teaches the N-number of the first multiplexers include an odd-numbered multiplexer performs time- division on odd-numbered pixel data in response to an inputted first selection control signal to output the time-divided data, and an even-numbered multiplexer performs time- division on even-numbered pixel data in response to an inputted second selection control signal to output the time-divided data (figs. 4-5,items 100,300, col. 4, lines 27-60 and col. 5., lines 60-67).

As to claims 9,11 Jeong teaches the first and second selection control signals have a logical state opposite to each other, and the logical state is inverted at least for each half or quarter horizontal period (col. 1, lines 42-46).

As to claims 14,16 Kim and Lee do not disclose one horizontal period is divided into two half horizontal periods and the pixel data are time-divided to be supplied.

Jeong teaches one horizontal period is divided into multiple horizontal periods and the pixel data are time-divided to be supplied (fig.6, col. 5, lines19-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Jeong into Lee and Kim system in relation to two halves of horizontal periods in order to reduce number of components (col. 2, lines 51-52 in the Jeong reference).

Allowable Subject Matter

4. Claims 5-6,10,12,15,17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 5 the major difference between the teaching of the prior art of record (Kim and Lee) and the instant invention is that a second multiplexer array for determining a progress path of the time-divided pixel data in response to an input polarity control signal to make the time-divided pixel data inputted to at least an N-number of positive and negative digital-to-analog converters among at least the N-number of positive and negative digital-to-analog converters; and a third multiplexer array for determining a progress path of the pixel voltage signal in response to the polarity control signal to make the pixel voltage signal inputted to the demultiplexer array.

Claim 6 depends on claim 5.

Relative to claims 10,12 and 15,17 the major difference between the teaching of the prior art of record (Kim, Jeong and Lee) and the instant invention is that the digital-to-analog converter array generates the pixel voltage signal in use of the pixel voltage signal level having a voltage at least one step higher in absolute value than the original pixel voltage signal level in correspondence to the pixel data outputted during the first half of one horizontal period, and generates the pixel voltage signal in use of the original pixel voltage signal level in correspondence to the pixel data outputted during the second half of the one horizontal period.

Response to Arguments

5. Applicant's arguments filed 05/27/08 have been fully considered but they are not persuasive:

On page 8, 1st paragraph of Remarks, Applicant's stated that "Kim" and "Lee", analyzed singly or in combination, do not teachat least this combination of features. First, claim 1 recites "the pixel data including even pixel data (RGB even) and odd pixel data (RGB odd)". Both "Kim" and "Lee" do not teach at least the feature of claim 1. Thus, none of the cited references, singly or in combination, teaches or suggests at least the feature of claim 1. However, as well known in the art any pixel data will including even pixel data (in Lee reference fig. 7, item D2) and odd pixel data (in Lee reference fig. 7, item D1) and Kim teaches RGB data (fig. 2).

On the same page , 1st paragraph of Remarks, Applicant's stated that claim 1 recites "a digital-to-analog converter array for converting the time-divided pixel data signals into pixel voltage signals". However, "Kim" does not disclose at least the feature of claim 1. See Fig. 2, item 39, col. 3, lines 40-57. "Kim" discloses "a decoder 39 for selectively outputting one of the 128 analog voltages supplied by an R-ladder and corresponding to output of the multiplexer 37". One of the 128 analog voltages is not time-divided pixel data signals corresponding to the feature of claim 1. Thus, Applicant submits that "Kim" and "Lee", analyzed singly or in combination, do not teach at least the feature of claim 1. However, in Kim reference D/A converter is a combination of items 37,39,41 which receives a digital RGB pixel value and output analog value (see correspondent description).

On page 8, 1st paragraph of Remarks, Applicant's stated that In particular there is no teaching in Lee wherein the digital to analog converter "generates a first pixel voltage signal level having a first voltage value corresponding to the first time-divided pixel data signal, generates a second pixel voltage signal level having a voltage at least one-step higher in absolute value than the first pixel voltage signal level and corresponding to the first time-divided pixel data signal.

However, Kim teaches structure of LCD driver with digital signal supplied from the multiplexer to digital-to analog converter, which will supply any values (fig. 2, items 37,39, 41 and correspondent text) and Lee teaches voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data (fig.7, item 400,col. 8, lines 52-63 and col. 12. lines 1-31). In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The same will apply to the arguments in relation to independent claims 13.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. S./
Examiner, Art Unit 2629
08/20/08

/Richard Hjerpe/

Supervisory Patent Examiner, Art Unit 2629